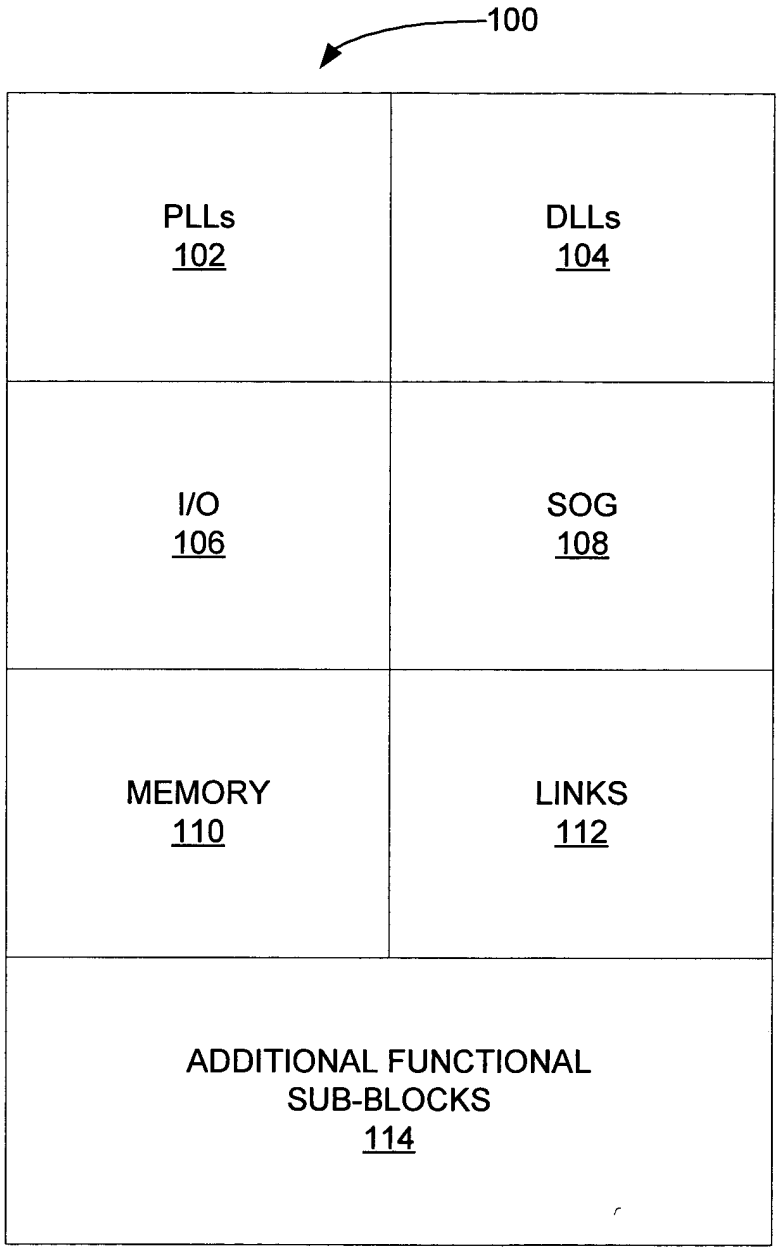
100
PLLs
102
DLLs
104
I/O
106
SOG
108
MEMORY
110
LINKS
112
ADDITIONAL FUNCTIONAL
SUB-BLOCKS
114

Figure 1

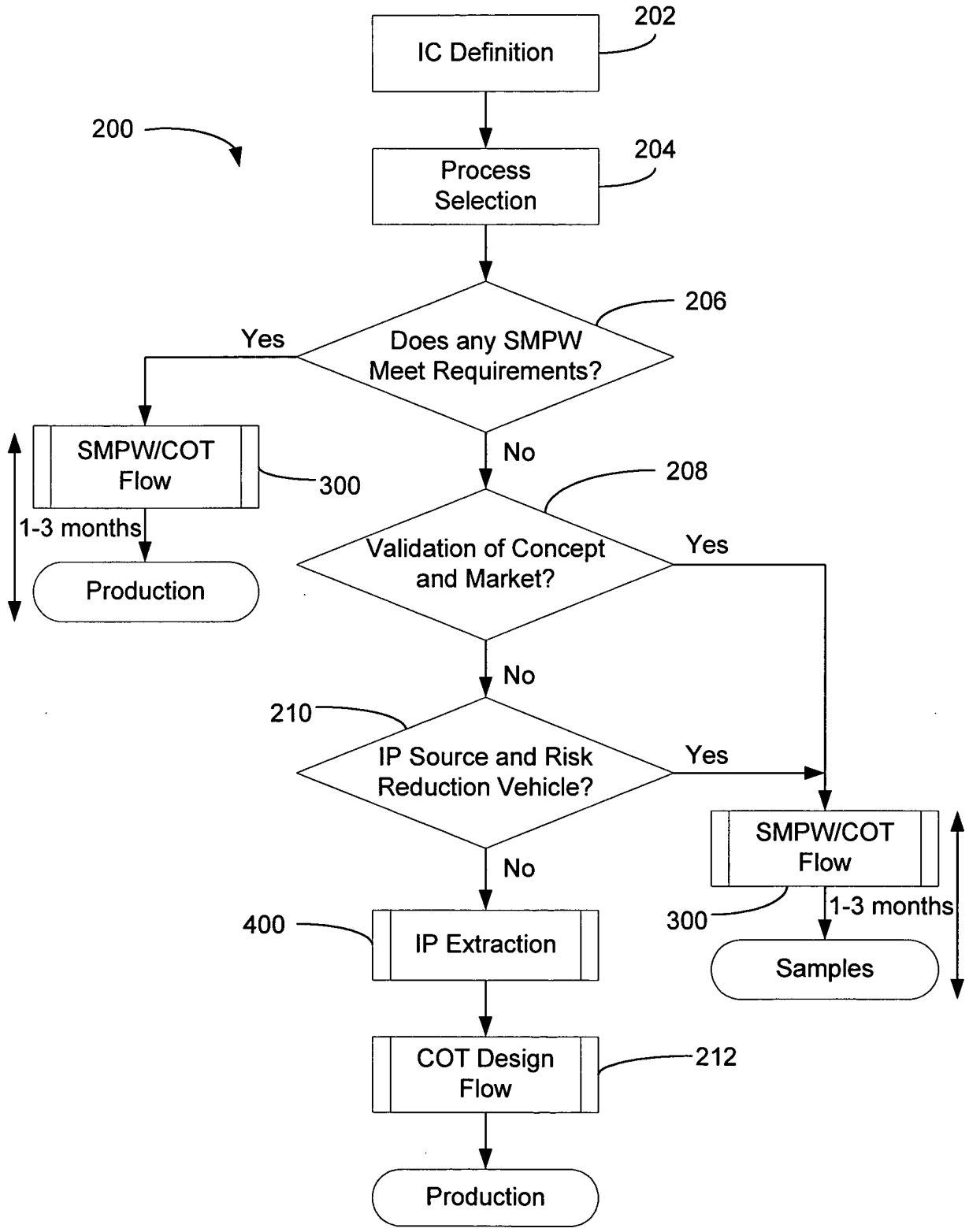
200
IC Definition
202
Process Selection
204
Does any SMPW Meet Requirements?
206
Yes
No
SMPW/COT Flow
300
1-3 months
Production
Validation of Concept and Market?
208
Yes
No
IP Source and Risk Reduction Vehicle?
210
Yes
No
SMPW/COT Flow
300
1-3 months
Samples
400
IP Extraction
COT Design Flow
212
Production

Figure 2

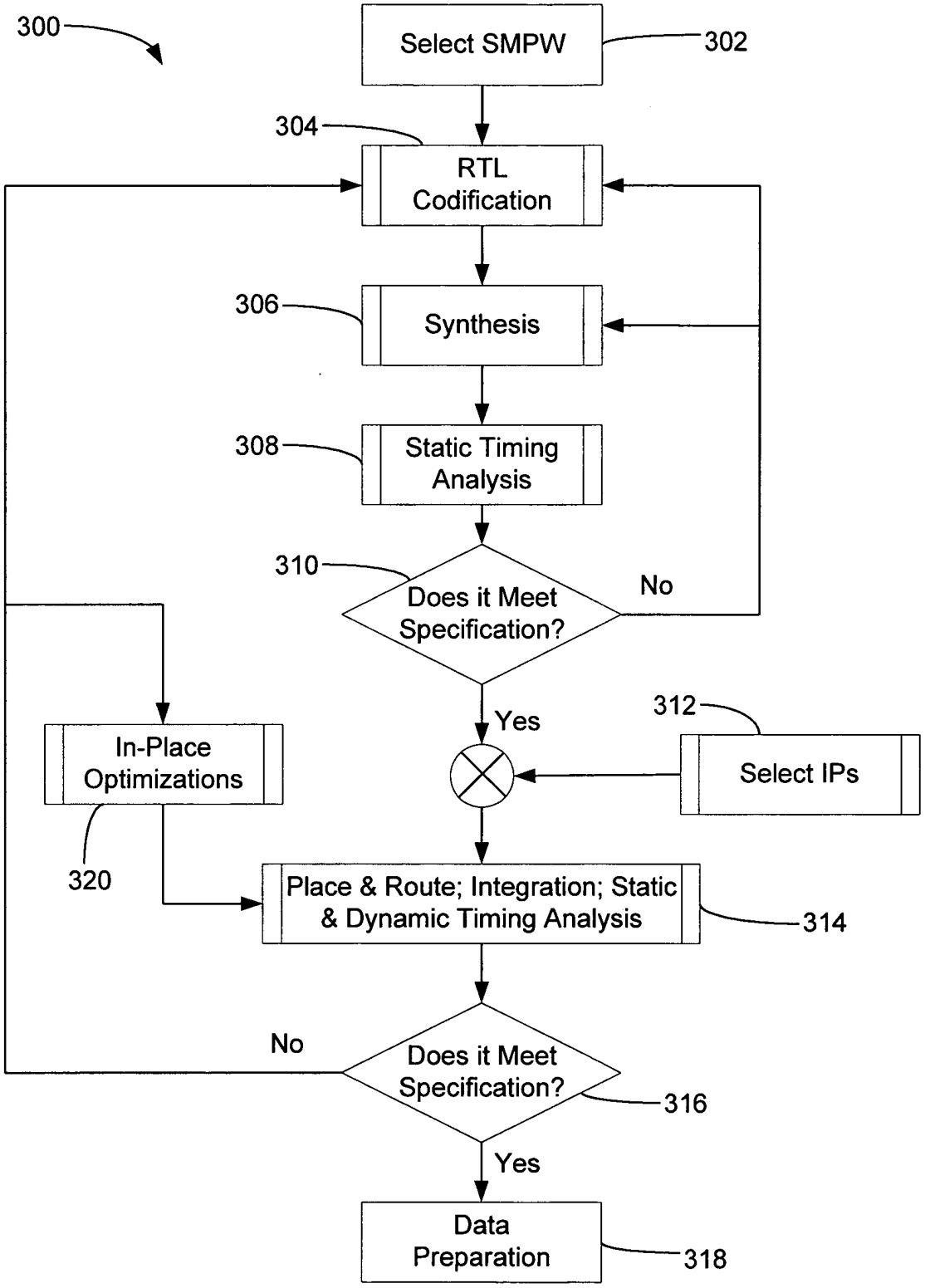
300
Select SMPW
302
304
RTL Codification
306
Synthesis
308
Static Timing Analysis
310
Does it Meet Specification?
No
Yes
312
Select IPs
In-Place Optimizations
320
Place & Route; Integration; Static & Dynamic Timing Analysis
314
No
Does it Meet Specification?
316
Yes
Data Preparation
318

Figure 3

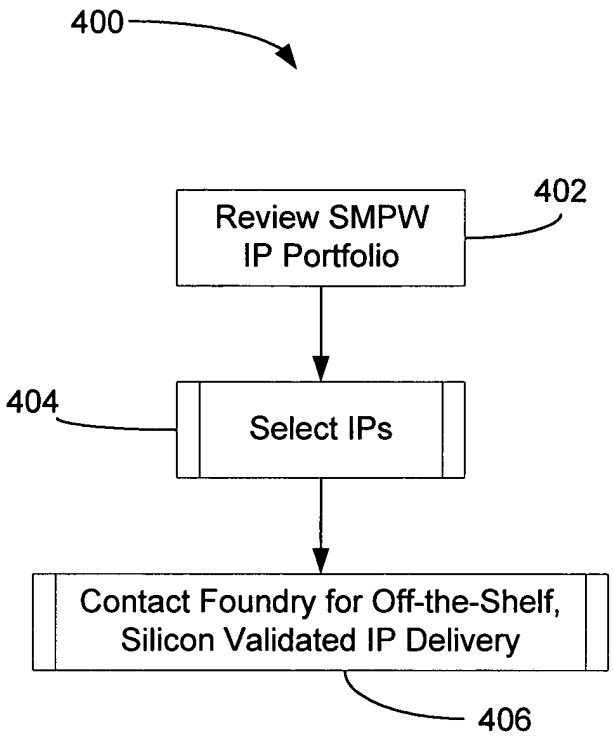
400
Review SMPW IP Portfolio
402
404
Select IPs
Contact Foundry for Off-the-Shelf, Silicon Validated IP Delivery
406

Figure 4